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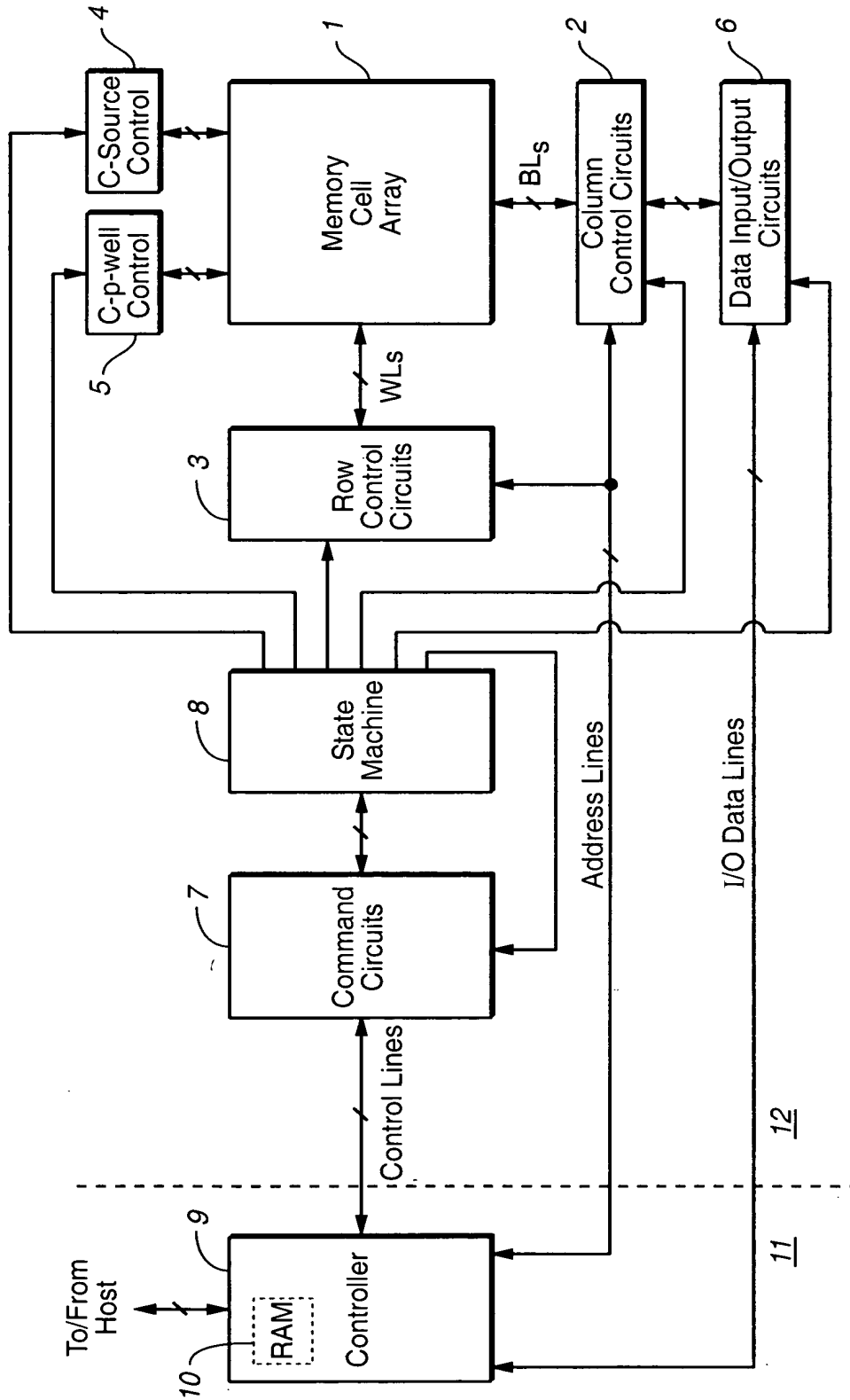
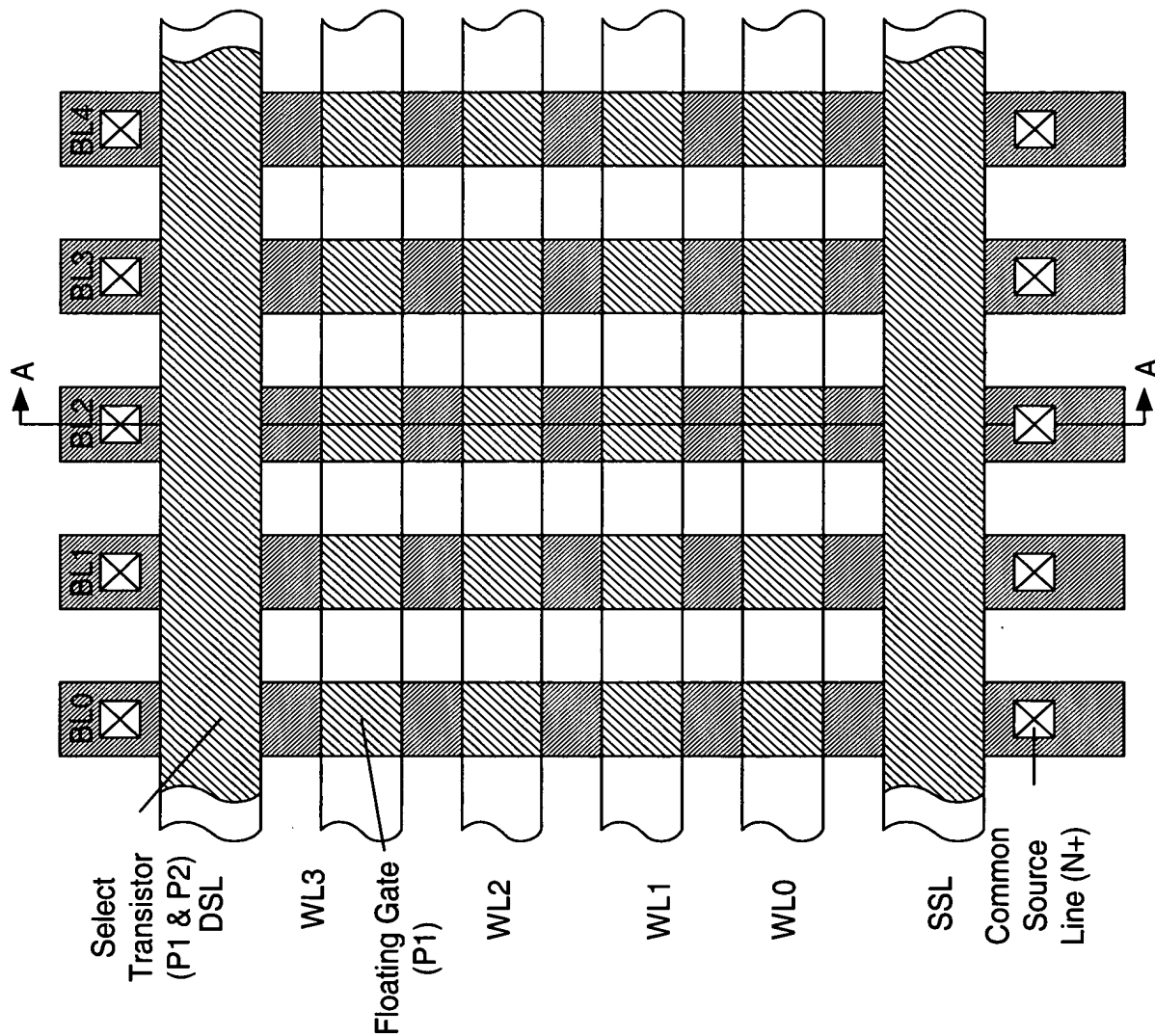
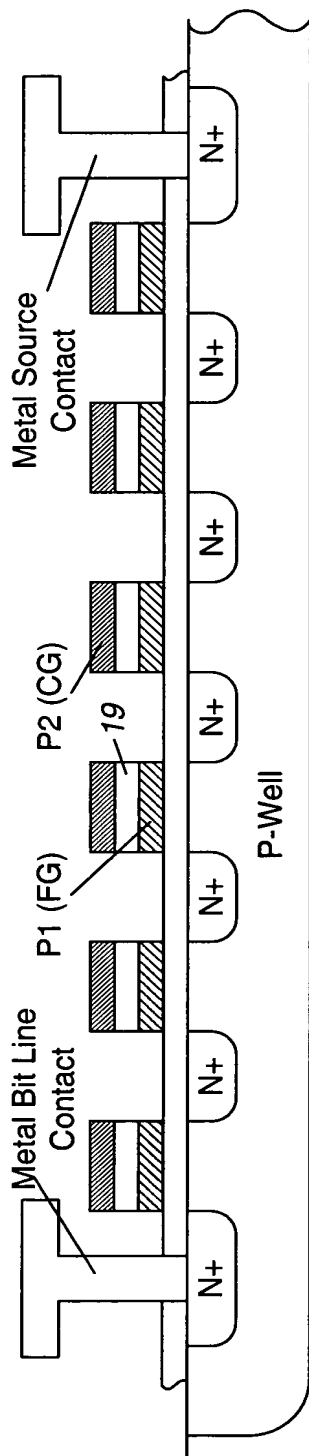


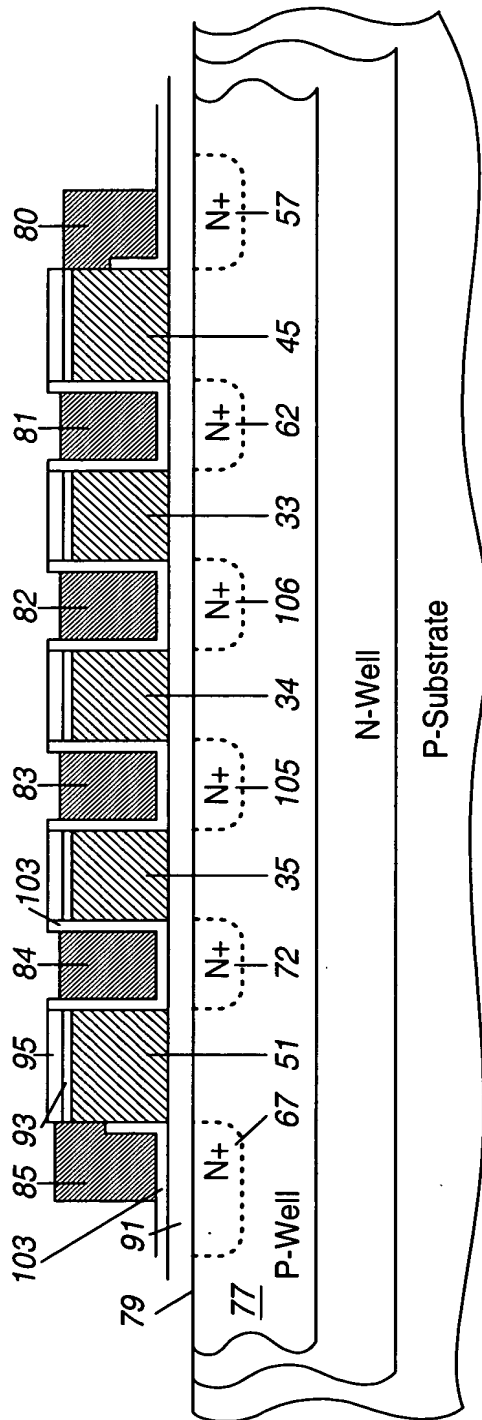
FIG. 1



**FIG. 2A (PRIOR ART)**



**FIG. 2B** (PRIOR ART)  
 (Section A-A)



**FIG. 4**  
 (Section A-A)

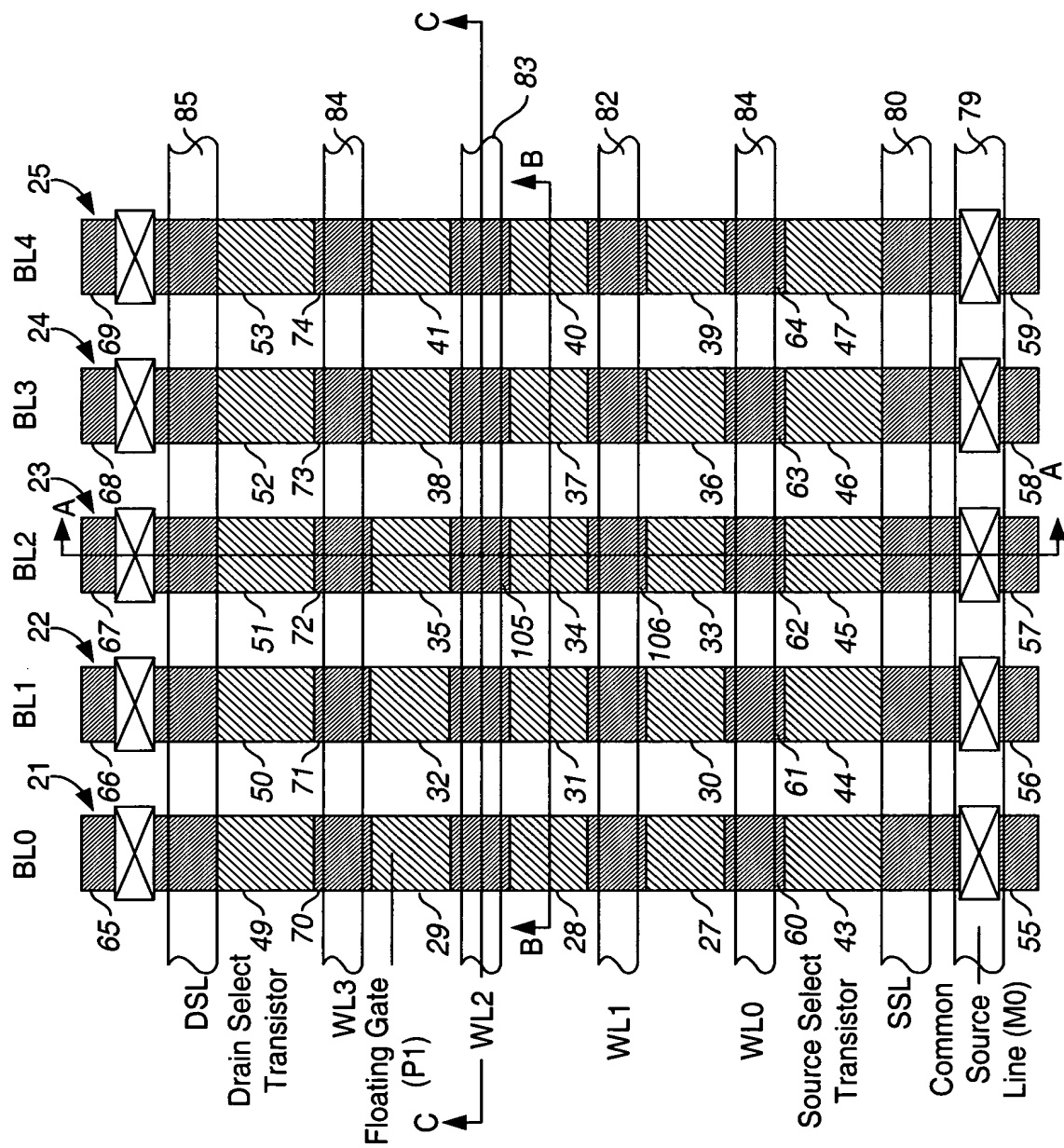
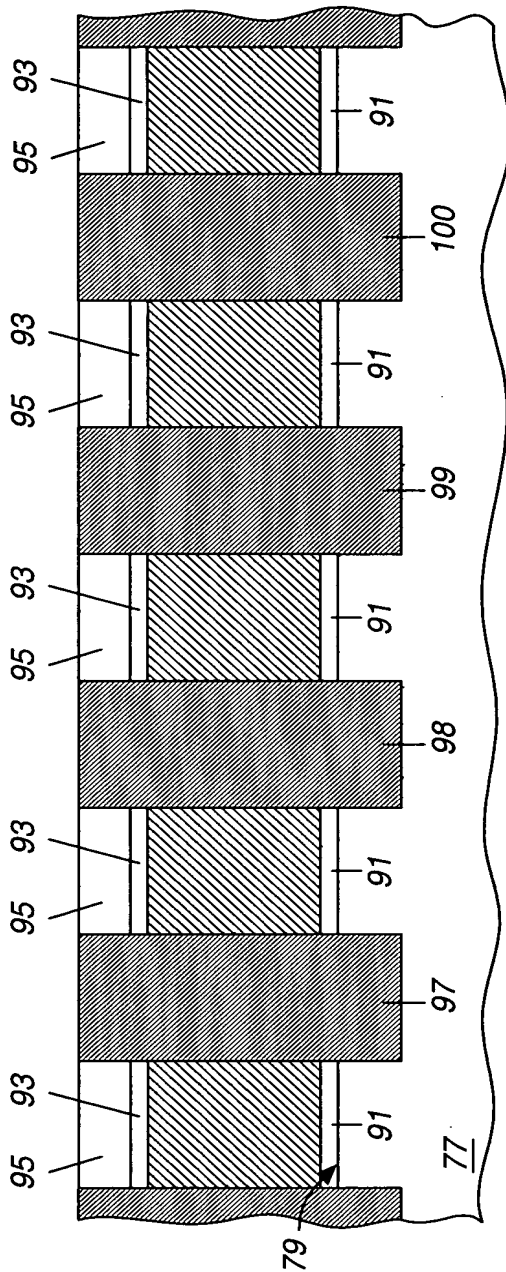
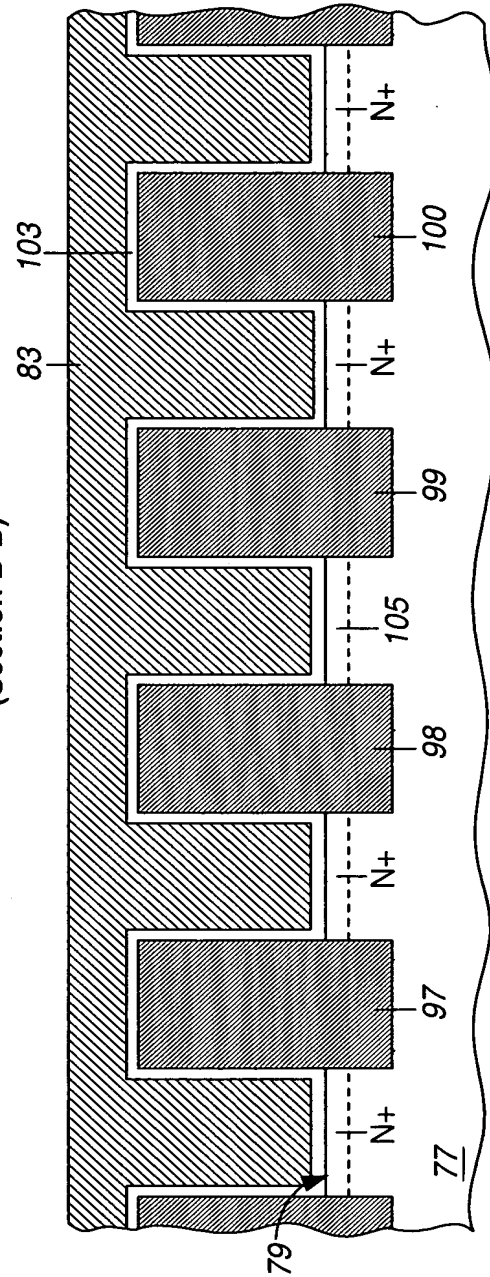


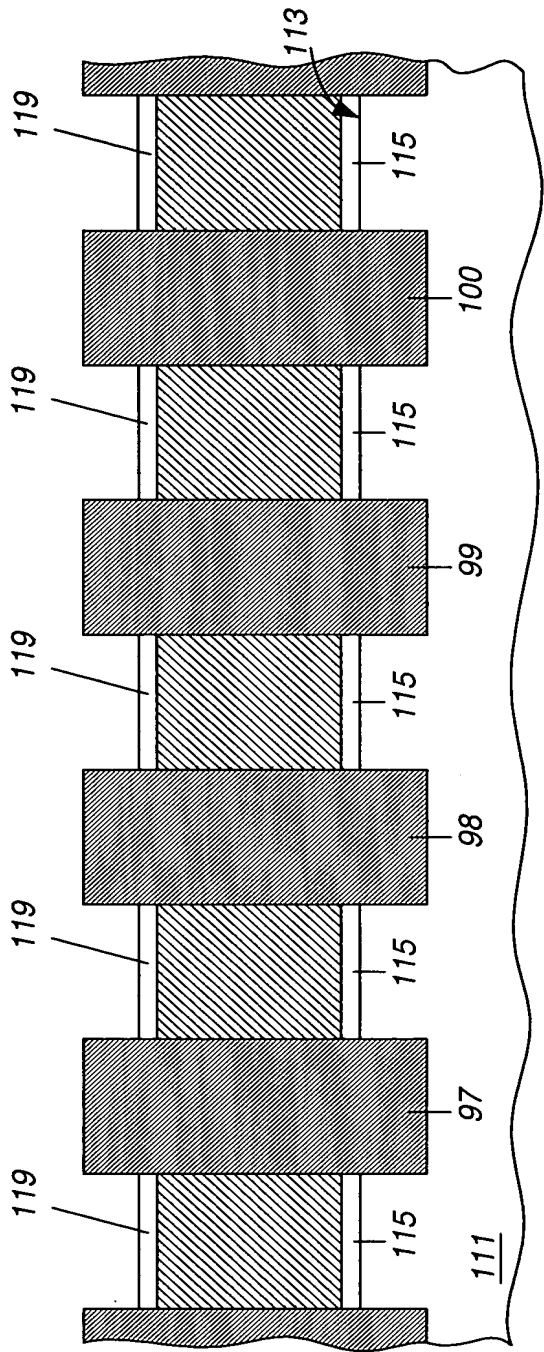
FIG. 3



**FIG. 5A**  
(Section B-B)



**FIG. 5B**  
(Section C-C)



**FIG. 6**  
(Section B-B)

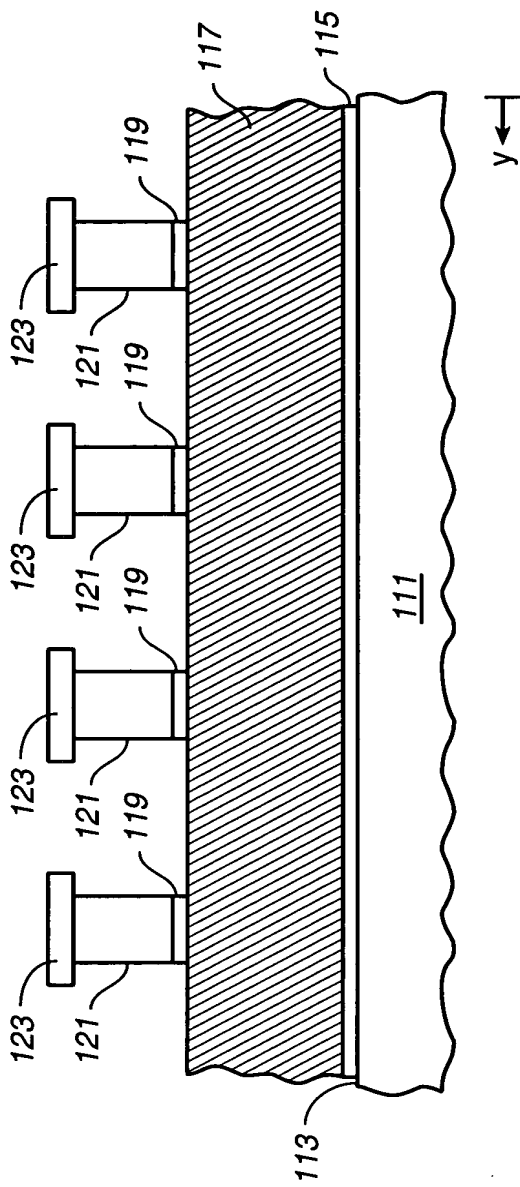


FIG. 7

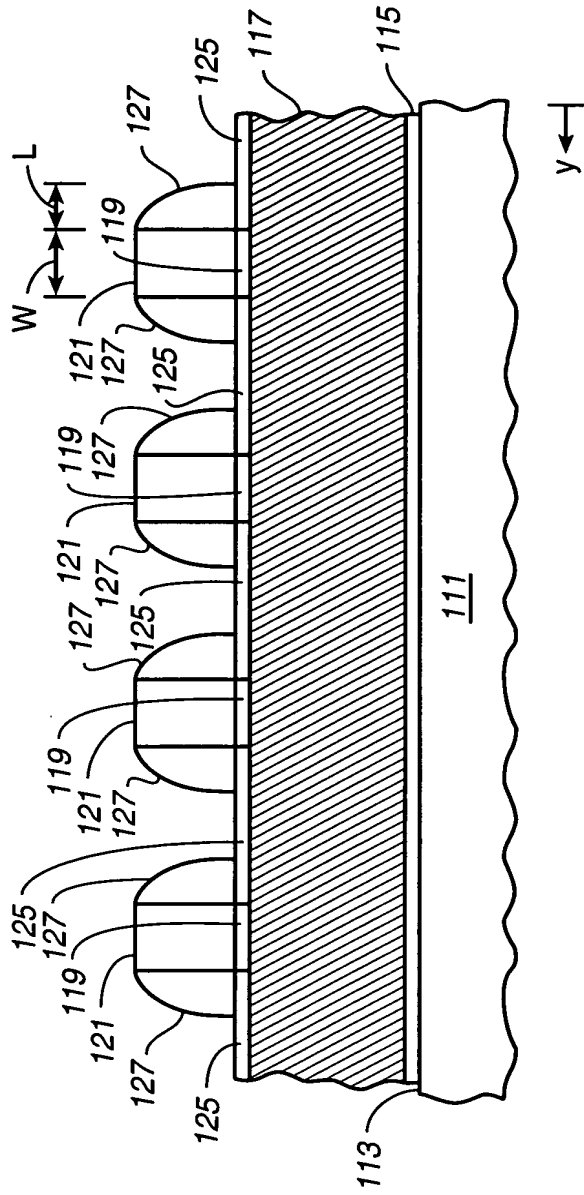


FIG. 8

FIG. 9

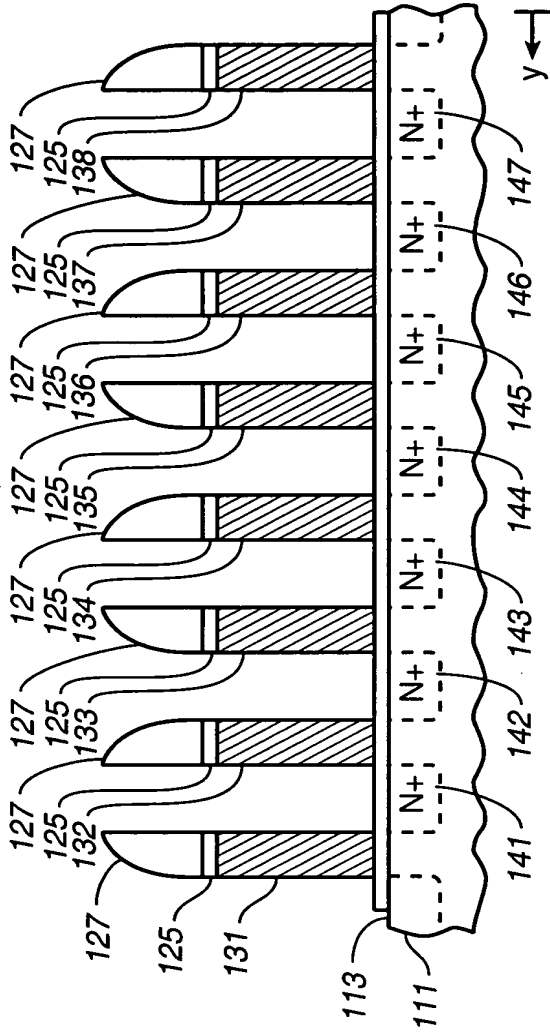
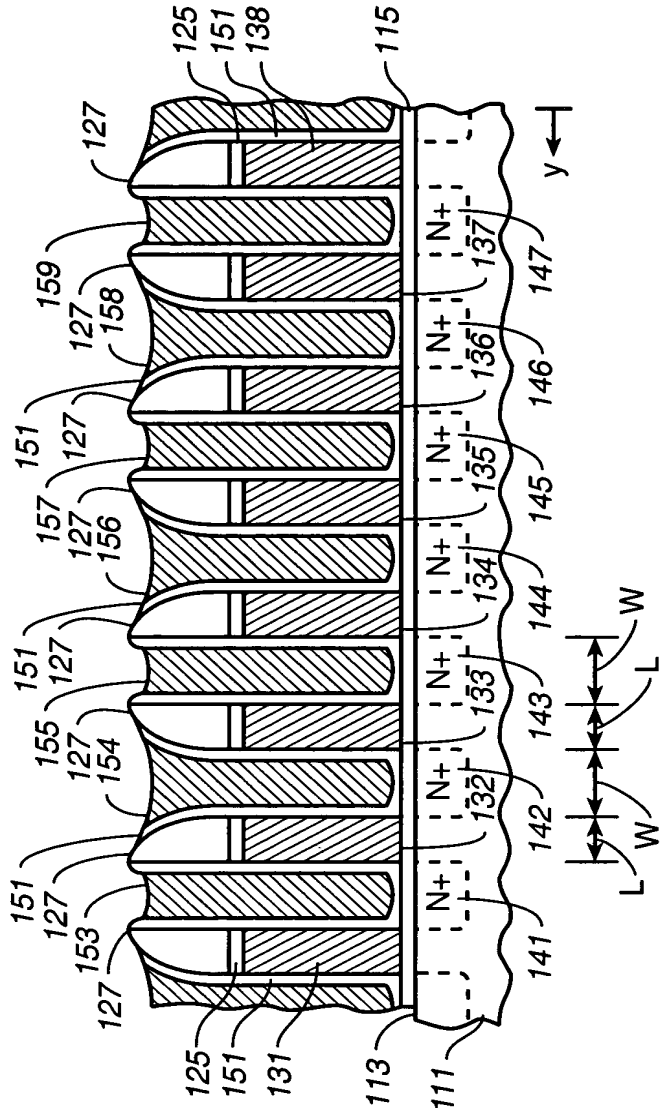


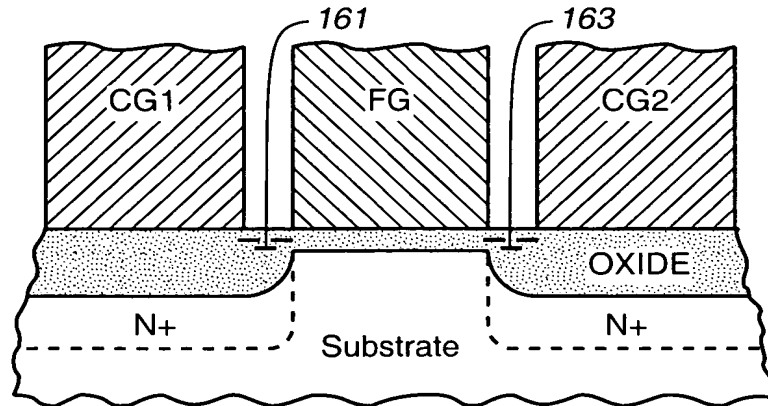
FIG. 10



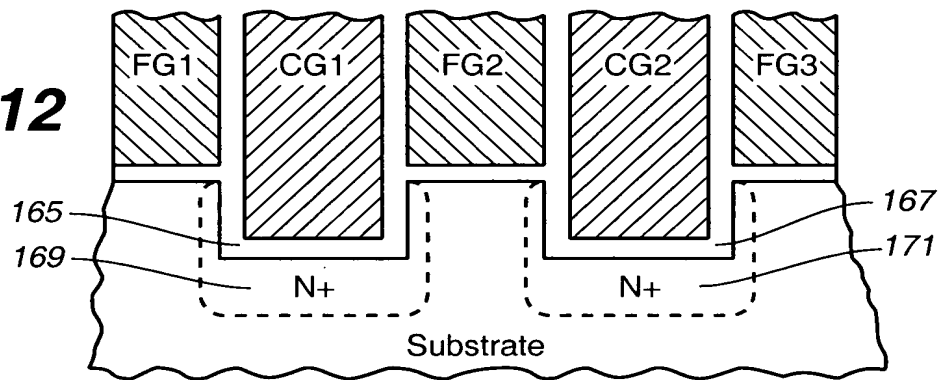


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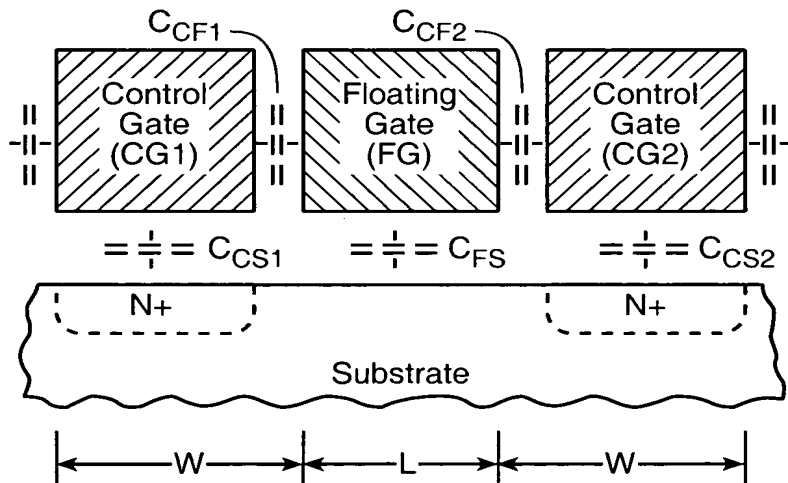
**FIG.\_11**



**FIG.\_12**



**FIG.\_13**



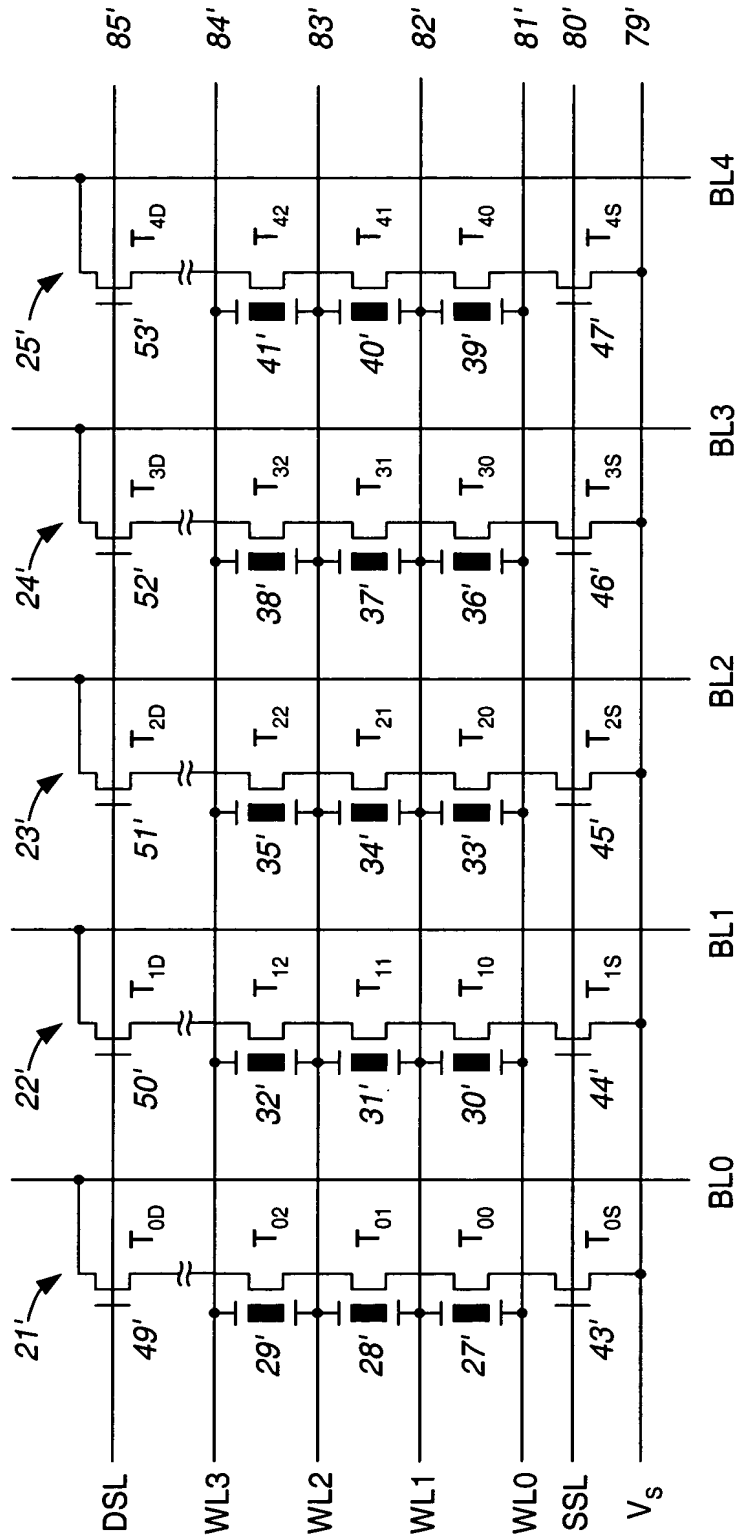


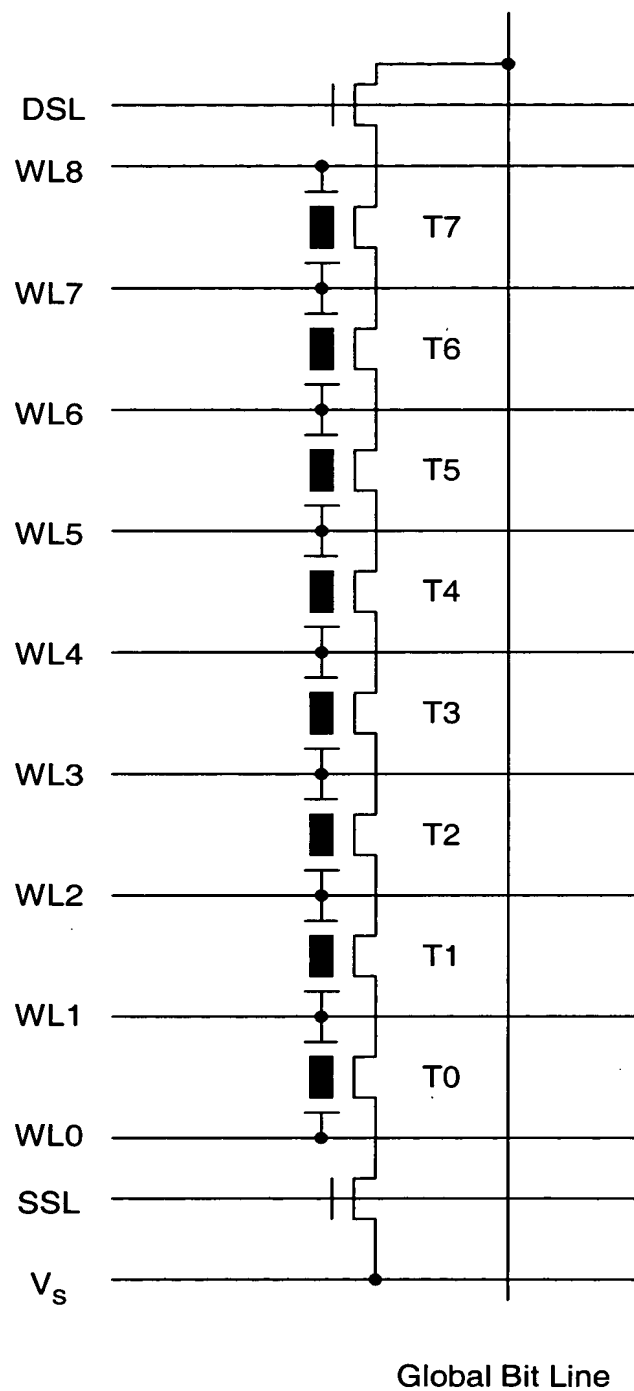
FIG. 14

	Erase	Program	Read
V <sub>D</sub> (bit lines)	Float	Program: 0v Pgm Inhibit: ~2v	sensed
V <sub>SSL</sub>	Float	~2v	~5v
V <sub>S</sub>	Float	0 v, Float, or slight positive	0v
P-Well	~16v	0 v	0v
V <sub>CG</sub> : (all control gates)	0v – selected block Float - unselected	-	-
Selected cell (both gates)	-	~13 – 20 v stepped	0 – 5 v stepped
All unselected cells (above selected cell)	-	~2v	~5v <sup>(1)</sup>
All unselected cells (below selected cell)	-	~0v	~5v <sup>(1)</sup>

FIG.\_ 15

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**FIG. 16**